REMARKS

Claims 1 - 19 are pending in the present application. By this Amendment, claim 1 has been amended. No new matter has been added. It is respectfully submitted that this Amendment is fully responsive to the Office Action dated November 1, 2004.

Regarding Claim Rejections – 35 U.S.C. § 102

Claims 1-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Eklund *(U.S. Patent 5,506,158)*.

This rejection is respectfully traversed.

Claim 1 is amended so as to definitely claim that the step of patterning the semiconductor film to form the resistance element and the gate electrode is performed before any step of implanting any dopant to be implanted into the gate electrode. This amendment to claim 1 makes it clear that the semiconductor film to be patterned into the gate electrode is not implanted not only with the dopant which is the same as that implanted in the first region where the resistance element is to be formed, but also any other dopant to be implanted in the gate electrode when the step of patterning the semiconductor film is performed.

In Eklund, as discussed in the previous response, areas of polysilicon layer 29 where the PMOS gate and the p-type resistor are to be formed are implanted with an p-type dopant (column 3, lines 59-63, FIG. 2D) and then areas of the polysilicon layer 29 where the emitter and the NMOS gate are to be formed are implanted with an n-type dopant (column 3, lines 64-67 and

column 4, lines 1-3, FIG. 2E). After the resistor and PMOS and NMOS gates have been doped, the polysilicon layer 29 is patterned and etched to form the emitter electrode 30, gates 40 and resistor 70 (column 4, lines 1-3, GIG. 2F).

Regarding both of the PMOS and NMOS gates in Elklund, the polysilicon layer 29 is doped with a dopant prior to the step of patterning the polysilicon layer 29 to form the gate electrode, while the Examiner argues in the section of Response to Arguments that the gates are doped at the same time that the source and drain regions are formed. It is clear the Eklund fails to disclose the step of patterning the semiconductor film to form the resistance element and the gate electrode before any step of implanting any dopant to be implanted into the gate electrode.

In the present invention according to claim 1, the step of patterning the semiconductor film to form the resistance element and the gate electrode is performed before any step of implanting any dopant to be implanted into the gate electrode, whereby it is possible to form the gate electrodes of transistors of different conduction types in the same configuration. Such a technical effect cannot be realized in Eklund in which both the areas of the semiconductor layer where the PMOS and NMOS gates are to be formed are implanted before the step of patterning the semiconductor film to form the gates.

As described above, Eklund fails to disclose all the features of the present invention according to claim 1, and it is clear that the present invention according to claim 1 cannot be anticipated by Eklund.

Claims 2-19 are directly or indirectly dependent from claim 1, and the present invention according to claim 1 cannot be anticipated by Eklund. Therefore, it is also clear that the present invention according to claims 2-19 cannot be anticipated by Eklund.

In view of the aforementioned amendments and accompanying remarks, Applicants submit that that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

WESTERMAN, HATTORI, DANIELS & ADRIAN, LLP

Thomas E. Brown
Attorney for Applicants
Registration No. 44,450

TEB/jl
1250 Connecticut Avenue, NW
Suite 700
Washington, D.C. 20036
(202) 822-1100 (t)
(202) 822-1111 (f)